Megaimpulse
MODERN SEMICONDUCTOR TECHNOLOGIES

Picosecond Pulse Generator Module for Antenna Arrays

PPM0732

- **Compact**
- **Extremely high voltage rise rate**
- **Low jitter**
- **Integrated PLL circuit for the exact synchronization within antenna array**

PPM0732 is based on Drift Step Recovery Diodes (DSRD) and Silicon Avalanche Shapers (SAS) - new types of semiconductor devices, which allow obtaining best-in-class voltage rise rate, high reliability, low jitter, and long operation lifetime. The pulse generator module is designed for the operation within phased antenna arrays and can be used in other applications where precise synchronization of many generators or other equipment is required. It is based on PPM0731 and includes an additional circuit that provides the exact synchronization of the output HV pulse with the falling edge of the triggering pulse. In this way, the temperature drift of the output pulse and fluctuations due to deviation of the components parameters or aging are eliminated. The output pulses of all the generators in the array can be synchronized with 10 ps accuracy. No additional adjusting or deskew procedures are required if the length of the cables is matched.

Pulse amplitude	6...7 kV (see Fig.2)
Pulse polarity, waveform	positive, bell-like
Pulse rise time	< 150 ps
Pulse width (FWHM)	< 400 ps
Max repetition rate	10 kHz (continuous)
Jitter (RMS)	< 20 ps
Jitter (peak-to-peak)	< 100 ps
Output connector	N type
Input triggering connector	SMA type
Triggering pulse	+5V, 165...172 ns width
Power supply	
low voltage	+24V DC; 0.3A
high voltage	+160V DC; 0.3A

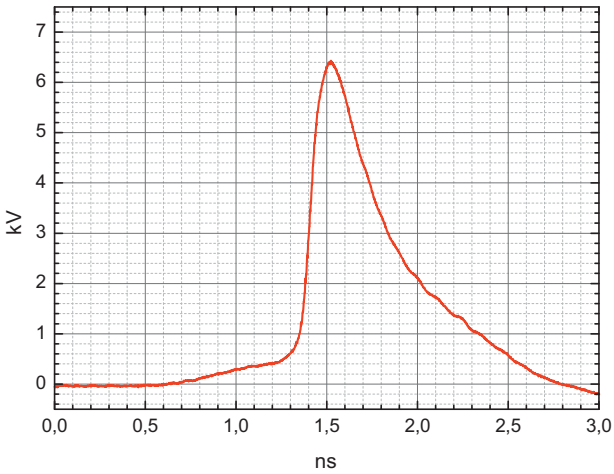
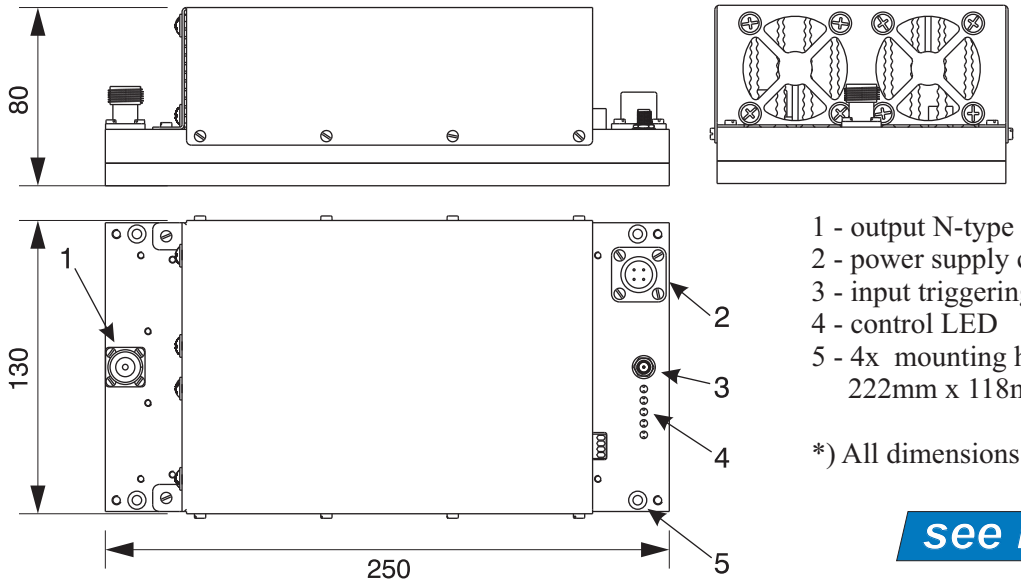


Fig.1. Typical output pulse waveform.



1 - output N-type connector
2 - power supply connector
3 - input triggering SMA connector
4 - control LED
5 - 4x mounting holes, 4.2mm dia, 222mm x 118mm footprint

*) All dimensions are in mm

see next page

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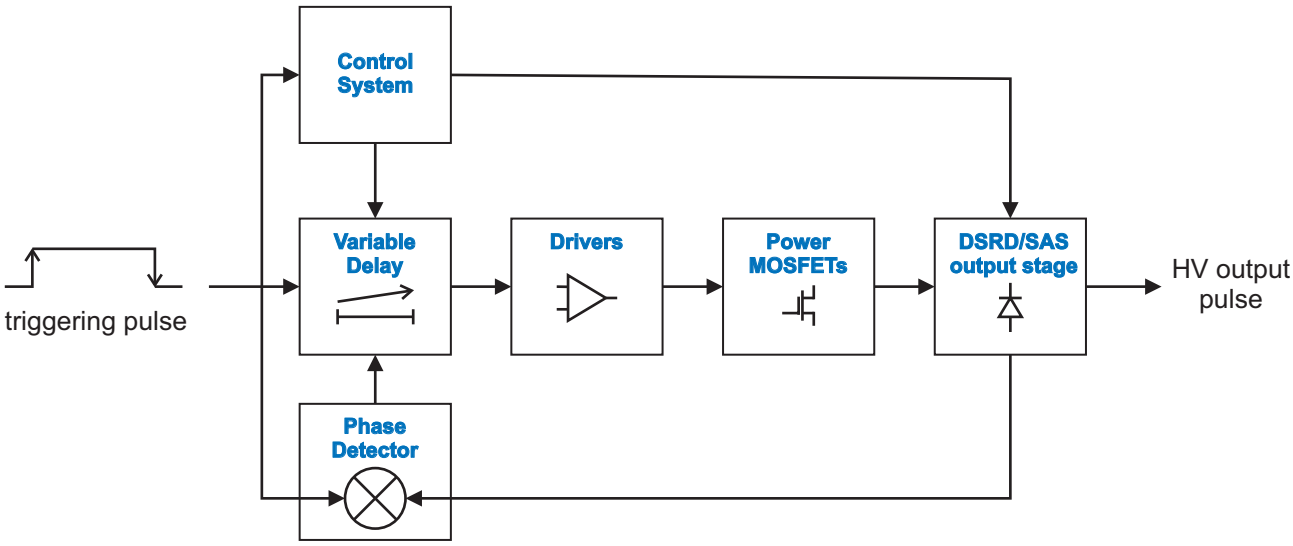

Fig.2. PPM0732 block diagram

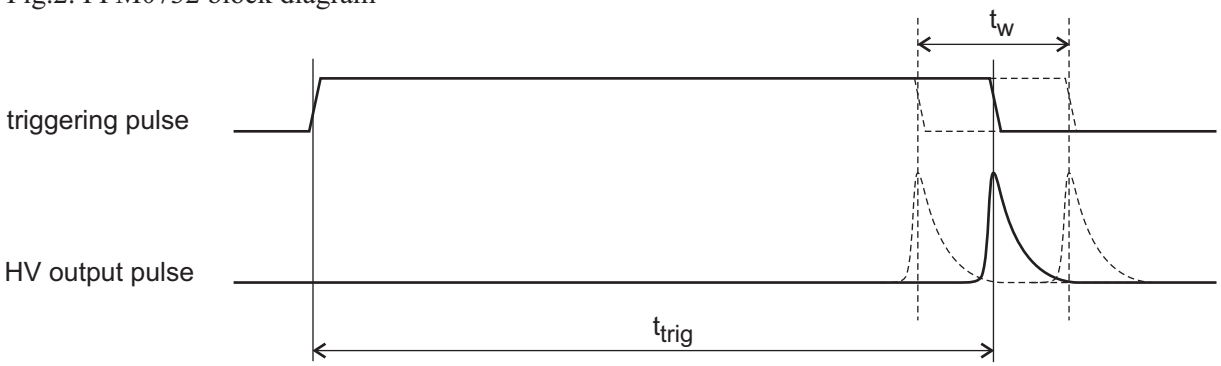

Fig.3. Output HV pulse synchronization with the triggering pulse falling edge

The operation principle of the synchronization system is clear from the PPM0732 block diagram in Fig.2 and the timing diagram in Fig.3. The key components are the phase detector and variable delay circuit. The phase detector compares the relative time position of the output HV pulse versus the trailing edge of the triggering pulse and variables the delay for the phase matching. In other words, the phase detector and variable delay circuit work as phase locked loop (PLL), which ensures the exact synchronization of the output HV pulse with the trailing edge of the triggering pulse. Few hundred pulses usually are required for the complete phase locking. The triggering pulse width t_{trig} should be within 165 ns ... 172 ns because the phase capture window t_w is 7 ns only, which is enough for the synchronization.
The other parameters are similar to PPM0731. Please look PPM0731 datasheet for more info.

PPM0732 delivery set includes:

1. PPM0732 pulse generator module.
2. PS601 fixed DC power supply voltage AC-DC converter.
3. N-SM141(50)-open semirigid 50 cm length output cable assembly with one N-type connector.
4. SMA-RG316(100)-SMA 100 cm length cable assembly with SMA connectors for the triggering pulses feeding.

Accessories:

1. PI-5/100 pulse inverter.
2. N-SM141(50)-N semirigid 50 cm length output cable assembly with two N-type connectors.