Megaimpulse
MODERN SEMICONDUCTOR TECHNOLOGIES

Picosecond Pulse Generator Module for Antenna Arrays

PPM0732

- **Compact**
- **Extremely high voltage rise rate**
- **Low jitter**
- **Integrated PLL circuit for the exact synchronization within antenna array**

PPM0732 is based on Drift Step Recovery Diodes (DSRD) and Silicon Avalanche Shapers (SAS) - new types of semiconductor devices, which allow obtaining best-in-class voltage rise rate, high reliability, low jitter, and long operation lifetime. The pulse generator module is designed for the operation within a phased antenna array and can be used in other applications where precise synchronization of many generators or with other equipment is required. It is based on PPM0731 module and includes an additional Phase Locked Loop circuit that provides the exact synchronization of the output HV pulse time position with the trailing edge of the triggering pulse. In this way, the temperature drift of the output pulse and fluctuations due to variation or aging of the components' parameters are eliminated. A lot of PPM0732 modules can be synchronized in the array with 10 ps accuracy. No additional adjusting or deskew procedures are required in the properly designed and assembled antenna array.

Pulse amplitude	6...7 kV (see Fig.2)
Pulse polarity, waveform	positive, bell-like
Pulse rise time	< 150 ps
Pulse width (FWHM)	< 400 ps
Max repetition rate	10 kHz (continuous)
Jitter (RMS)	< 20 ps
Jitter (peak-to-peak)	< 100 ps
Output connector	N type
Input triggering connector	SMA type
Triggering pulse	+5V, 168...175 ns width
Power supply	
low voltage	+24V DC; 0.3A
high voltage	+160V DC; 0.3A

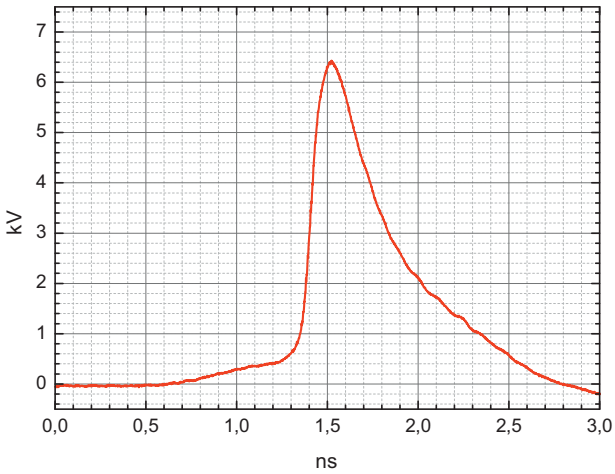
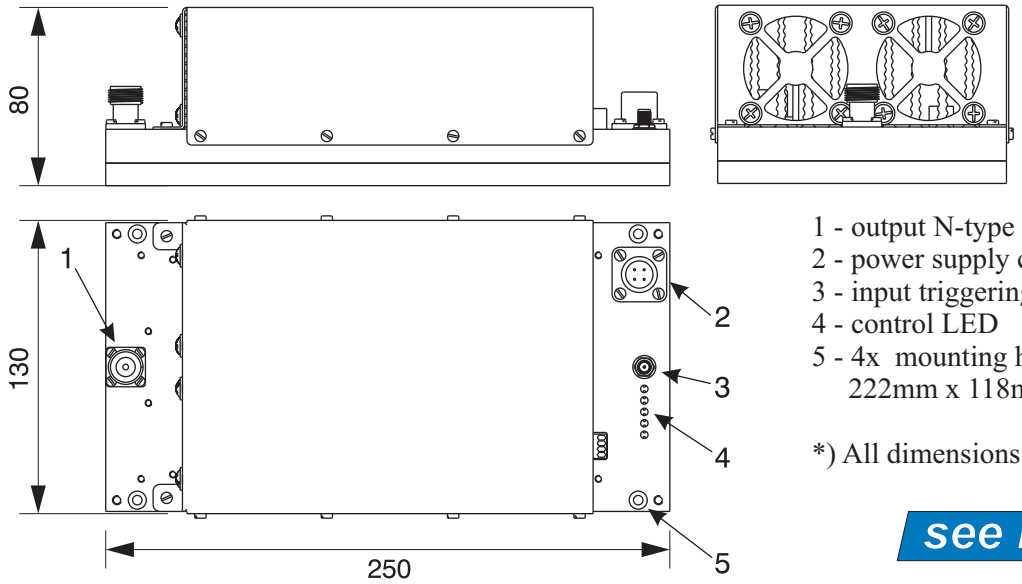


Fig.1. Typical output pulse waveform.



1 - output N-type connector
2 - power supply connector
3 - input triggering SMA connector
4 - control LED
5 - 4x mounting holes, 4.2mm dia, 222mm x 118mm footprint

*) All dimensions are in mm

see next page

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v1.0, February 09, 2022

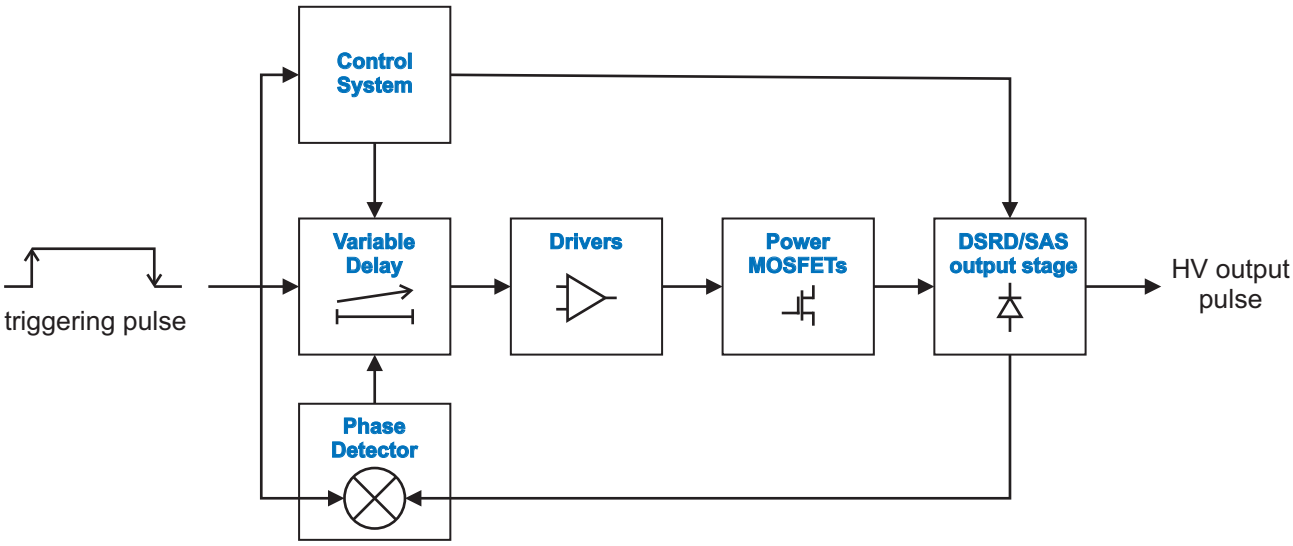

Fig.2. PPM0732 block diagram.

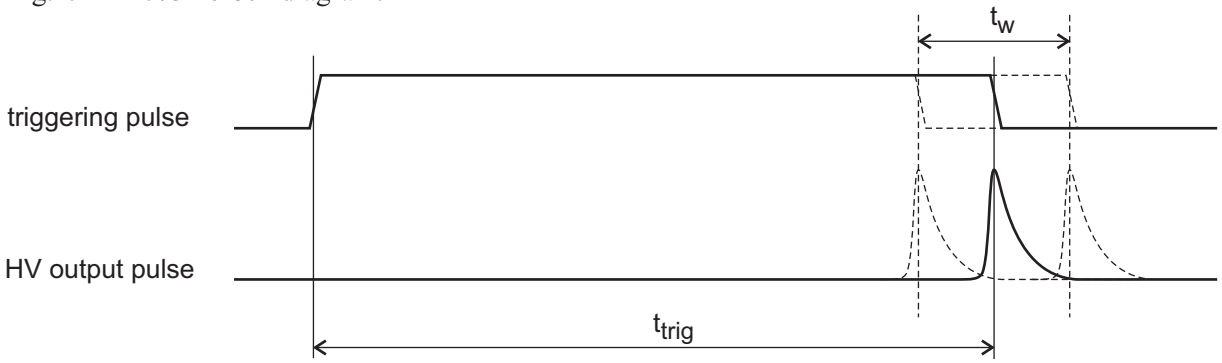

Fig.3. The timing diagram of HV output pulse synchronization with the trailing edge of the triggering pulse.

The operation principle of PPM0732 synchronization system is described in the block and timing diagram (Fig.2 and Fig.3). The key components are the phase detector and variable delay circuit. The phase detector compares the position in the time of the output HV pulse and the position of the trailing edge of the triggering pulse. The signal which is proportional to the time difference is integrated and applied to the variable delay circuit. In this way, the phase detector and variable delay circuit work together as a Phase Locked loop (PLL) circuit and ensure the synchronization of the output HV pulse with the trailing edge of the triggering pulse. A few hundred pulses are required for the exact phase locking. The triggering pulse width t_{trig} should be fixed and stay within 168 ns ... 175 ns because the phase capture window t_w is 7 ns only. In spite of the narrow capture window t_w, it is enough to eliminate the temperature and aging drift of the output pulse.
Therefore, the output pulse position becomes stable in time and does not depend on the heating and aging of HV components. The other technical parameters of PPM0732 are similar to those of PPM0731. Please see PPM0731 datasheet and User Manual for more info.

PPM0732 delivery set includes:

1. PPM0732 pulse generator module.
2. PS601 fixed DC power supply voltage AC-DC converter.
3. N-SM141(50)-open semirigid 50 cm length output cable assembly with one N-type connector.
4. SMA-RG316(100)-SMA 100 cm length cable assembly with SMA connectors for the triggering pulses feeding.

Accessories:

1. PI-5/100 pulse inverter.
2. N-SM141(50)-N semirigid 50 cm length output cable assembly with two N-type connectors.